a buried isolation layer in the semiconductor substrate extending across the active area; and

a link region in the semiconductor substrate coupling the well region and the buried isolating region;

wherein the link region extends laterally inward beyond the well region and toward the body region to define a spacing between the body region and the link region that establishes the first breakdown voltage.

7. The device of claim **1**, wherein:

the device isolating region includes a well and a contact region formed on the well;

the body region includes a well and a contact region formed on the well; and

a depletion region is formed between the device isolating region and the body region that reaches the contact region of either the device isolating region or the body region at the first breakdown voltage.

8. The device of claim **1**, wherein the device isolating region comprises:

one or more well regions in the semiconductor substrate and configured as a ring surrounding the active area;

a buried isolation layer in the semiconductor substrate extending across the active area; and

a further well region adjacent the ring and the buried isolation layer to define a spacing between the body region and the link region that establishes the first breakdown voltage.

9. The device of claim **1**, wherein the conduction path is configured such that the device is a laterally diffused metal-oxide-semiconductor (LDMOS) device, and wherein breakdown events occur at a location spaced from the conduction path.

10. The device of claim **1**, wherein the device isolating region is electrically tied to the drain region such that the drain region is clamped to the first breakdown voltage during a breakdown event.

11. An electronic apparatus comprising:

a substrate having a first conductivity type; and

a transistor disposed in the substrate, the transistor comprising:

a first semiconductor region having a second conductivity type;

a second semiconductor region having the first conductivity type;

a third semiconductor region having the second conductivity type, adjacent the first semiconductor region, and spaced from the second semiconductor region by the first semiconductor region; and

a fourth semiconductor region having the second conductivity type and defining an active area of the transistor in which the first, second and third semiconductor regions are disposed;

wherein the second and fourth semiconductor regions are configured to define a diode depletion region having a first breakdown voltage lower than a second breakdown voltage in the first semiconductor region.

12. The electronic apparatus of claim **11**, further comprising a fifth semiconductor region in the active area and having the second conductivity type, wherein the second semiconductor region comprises a first well on which the fifth semiconductor region is disposed and a second well adjacent the first well and spaced from the fourth semiconductor region to establish the first breakdown voltage.

13. The electronic apparatus of claim **12**, wherein the first well and the second well have different dopant concentration levels.

14. The electronic apparatus of claim **11**, wherein the fourth semiconductor region comprises an isolation well configured as a ring surrounding the active area and spaced from the second semiconductor region to establish the first breakdown voltage.

15. The electronic apparatus of claim **11**, wherein the fourth semiconductor region comprises a buried isolation layer in the substrate, extending across the active area, and spaced from the second semiconductor region to establish the first breakdown voltage.

16. The electronic apparatus of claim **11**, wherein the fourth semiconductor region comprises:

a well region in the substrate and configured as a ring surrounding the active area;

a buried isolation layer in the substrate extending across the active area; and

a link region in the substrate coupling the well region and the buried isolation layer;

wherein the link region extends laterally inward beyond the well region and toward the second semiconductor region to define a spacing between the second semiconductor region and the link region that establishes the first breakdown voltage.

17. The electronic apparatus of claim **11**, wherein:

the fourth semiconductor region includes a well and a contact region formed on the well; and

a depletion region is formed between the fourth semiconductor region and the second semiconductor region that reaches the contact region at the first breakdown voltage.

18. A method of fabricating a transistor, the method comprising:

forming a device isolating region of the transistor in a semiconductor substrate, the substrate having a first conductivity type, the device isolating region having a second conductivity type and defining an active area of the transistor;

forming a body region of the transistor in the active area, the body region having the first conductivity type; and

forming source and drain regions of the transistor in the active area, the source region being disposed on the body region, the source and drain regions having the second conductivity type;

wherein the device isolating region and the body region are spaced from one another to establish a first breakdown voltage lower than a second breakdown voltage in a conduction path between the source and drain regions.

19. The method of claim **18**, wherein forming the body region comprises:

implanting dopant of the second conductivity type in a first well region of the body region on which the source region is disposed; and

implanting the dopant of the second conductivity type in a second well region adjacent the first well region and spaced from the device isolating region to establish the first breakdown voltage.

20. The method of claim **19**, wherein the first well and the second well have different dopant concentration levels.

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